

# 2STIC

Next-generation internet at terabit speed:

SCION in P4

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[www.2stic.nl](http://www.2stic.nl)

# A new internet architecture in P4

- We implemented the SCION internet architecture in P4 for the Intel Tofino
- Determine feasibility of running a new architecture on switch hardware and evaluate performance



# SCION

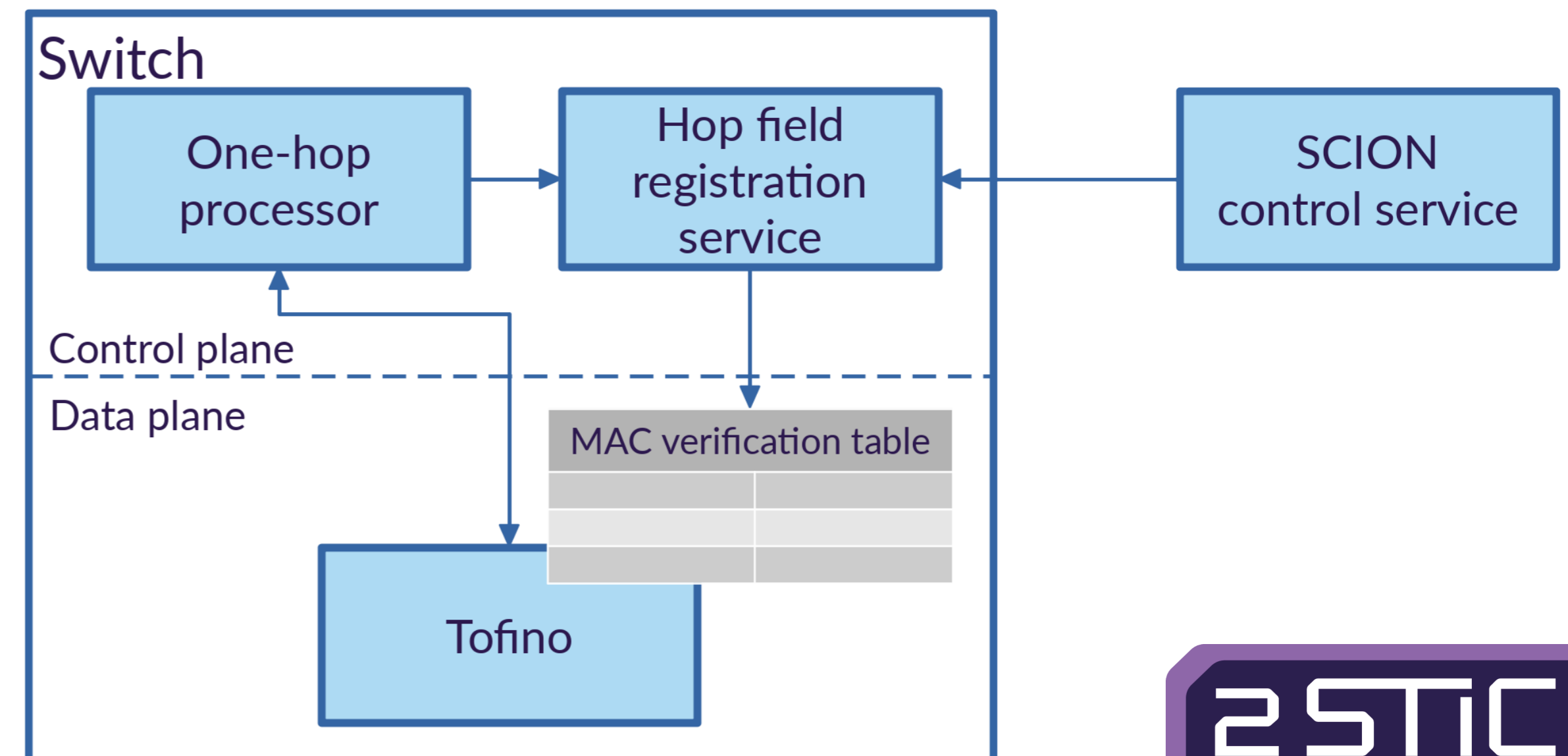
- Scalability, control, and isolation on next-generation networks
- Gaining momentum
- Path-aware networking
  - Paths contained in message headers
  - Authenticated using Message Authentication Codes (MACs)

# Some challenges

- No support for cryptographic operations in Intel Tofino
- Protocol not designed for hardware
  - Complex headers

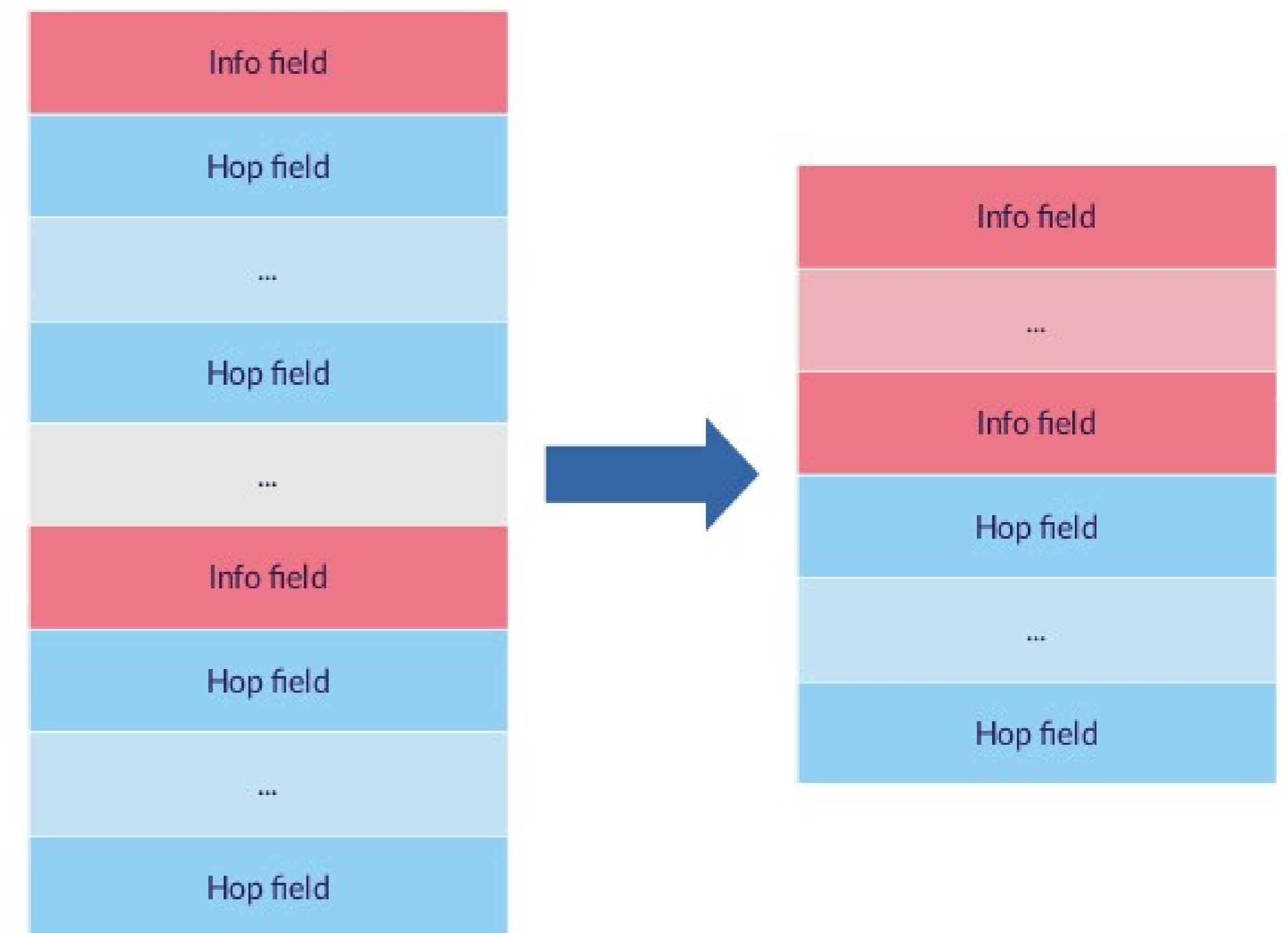
# No cryptographic operations

- MACs verified using table containing all currently valid values
- Populated from control plane when MACs are generated
  - In the SCION control plane
  - At the switch
- Invalid entries removed



# Complex header fields

- For example: forwarding path consisted of nested lists
- Flattening the structure provides for more efficient parsing

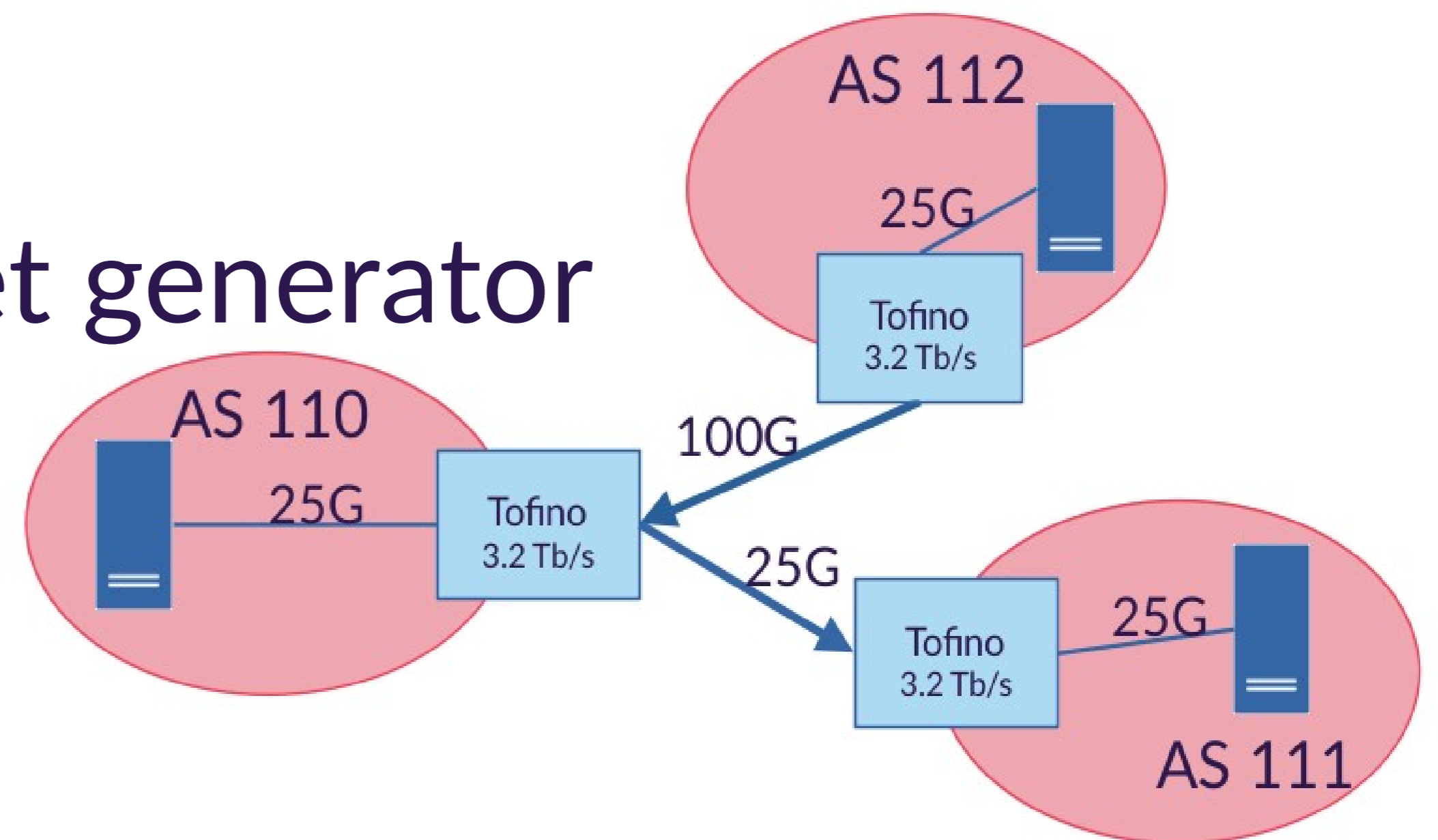


# Lessons learned

- When designing a protocol with hardware in mind
  - use explicit lengths
  - do not use absolute offsets
  - limit the usage of variable length fields
  - do not use complex data structures such as nested lists

# Evaluation

- Edgecore switches with 32 100 Gbps ports
- Tested functionality with topology where all border routers ran on switches
- Tested performance using packet generator for different path lengths
  - Achieved near line-rate for almost all tested path lengths





# Conclusion

- SCION can be implemented for switch hardware and run on high speeds
- Several lessons learned regarding protocol design
- Future work
  - Support for protocol error handling and additional SCION-related protocols
  - More extensive performance analysis

Code is open source and available at [github.com/SIDN/p4-scion](https://github.com/SIDN/p4-scion)