

2STIC

Implementation of SCION border router in P4 for Intel Tofino

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Security, Stability and Transparency in inter-network Communication

Put Dutch and European internet communities in leading position
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Introduction

- Goal: evaluate feasibility of running a future internet architecture like SCION directly on hardware

SCION

- No introduction necessary, I think



P4

“Programming Protocol-independent Packet Processors (P4) is a domain-specific language for network devices, specifying how data plane devices (switches, NICs, routers, filters, etc.) process packets.”

Source: <https://p4.org/>

Intel Tofino

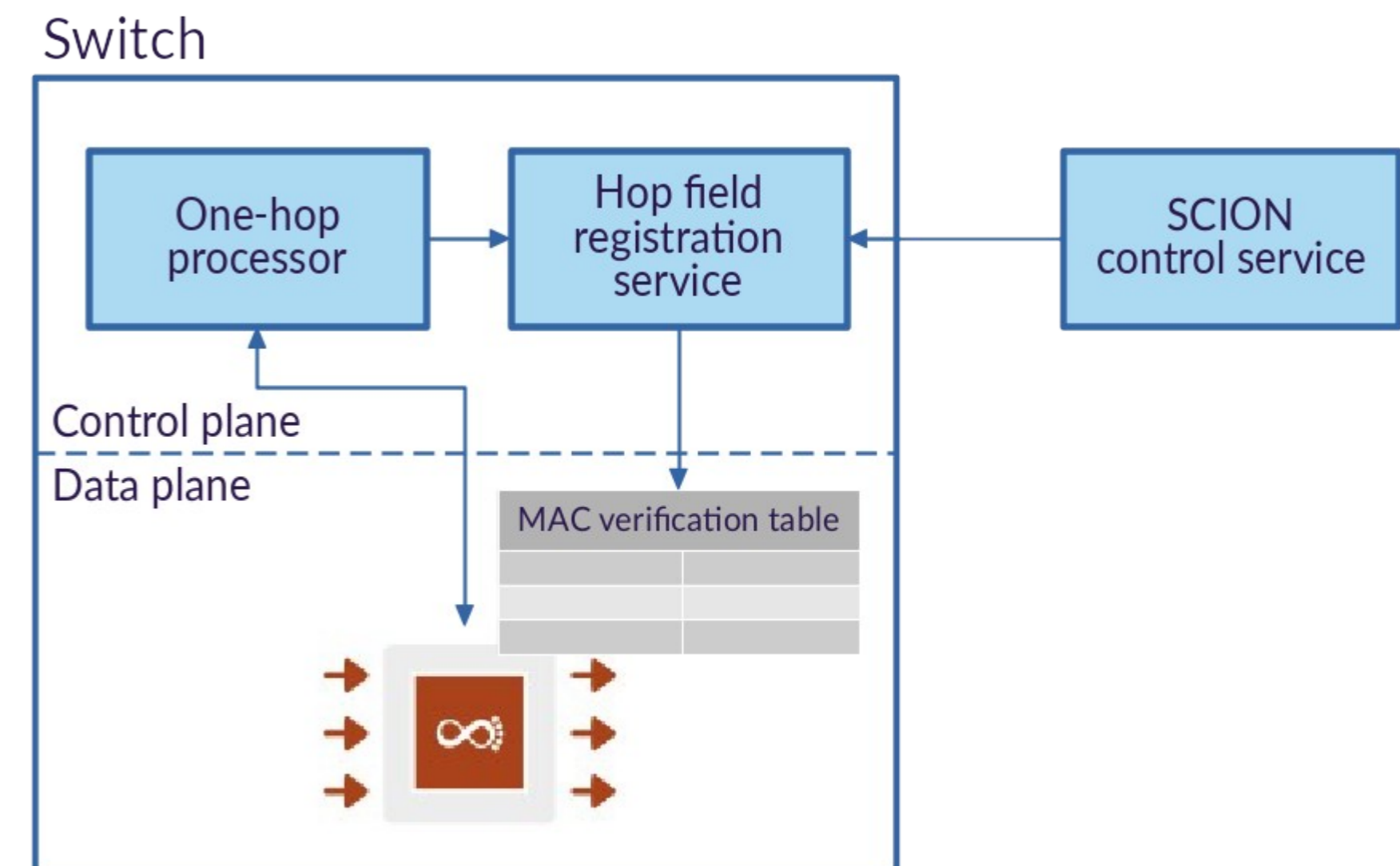
- P4-programmable Ethernet switch ASIC
- Switches available with e.g., 32 or 64 100 Gbit/sec ports

Implementation of prototype

- Cryptographic MAC
 - Changes to SCION headers
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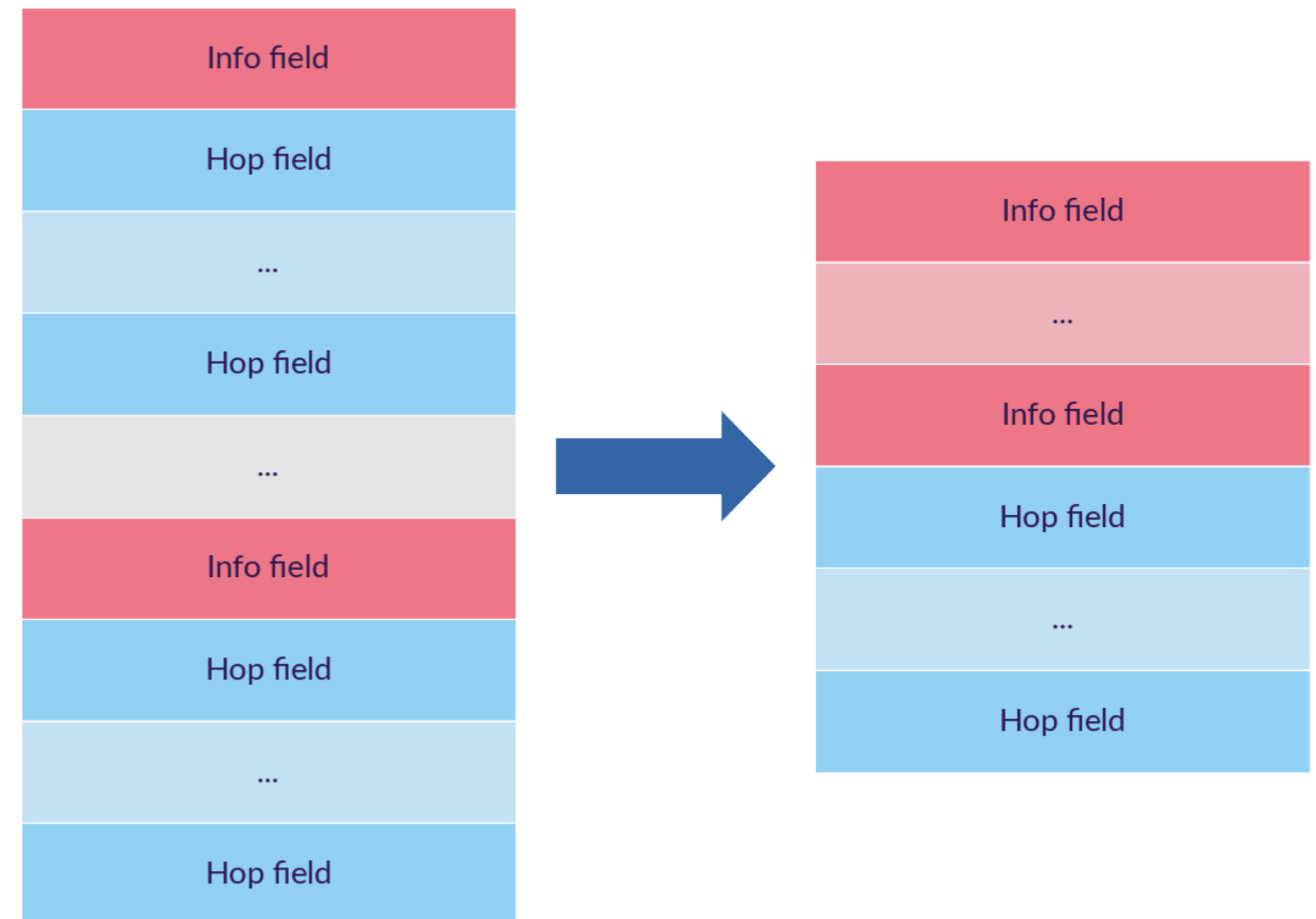
Cryptographic MAC

- Intel Tofino lacks support for cryptographic operations
- Hop fields
- Table
- Patched SCION control server
- Room for 160k-200k hop fields



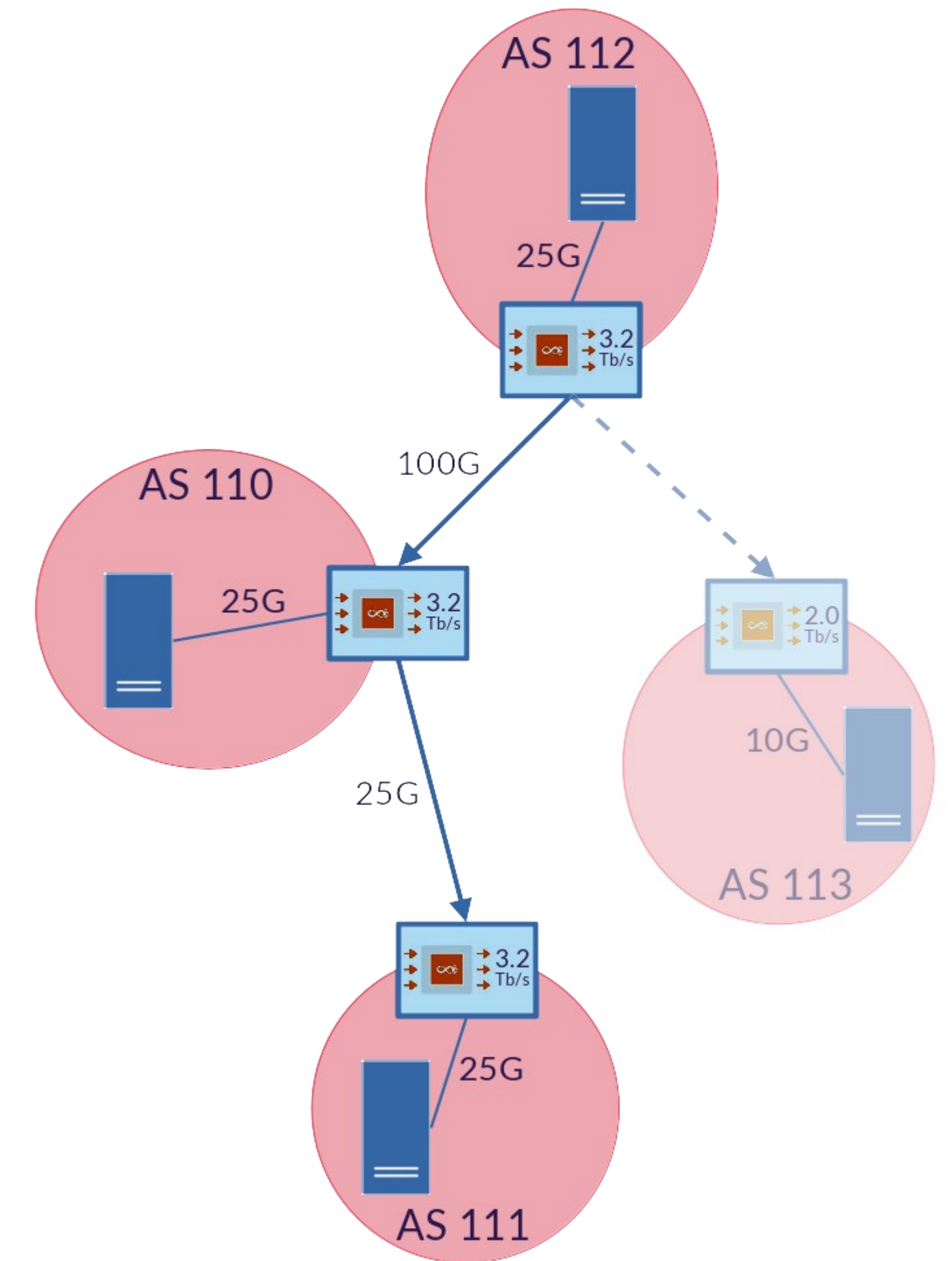
Changes to SCION headers

- Redesigned forwarding path
- Address types



Evaluation

- 2STiC testbed (<https://2stic.nl/testbed.html>)
- 3 ASs (4th being connected)



Future work

- Not implemented yet: peering, generation of SCMP error messages, ...
 - EPIC and COLIBRI: cryptographic MACs for individual packets
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Questions?

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